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EXAMINER				
CHERRY, STEPHEN J				
ART UNIT		PAPER NUMBER		
2863				
NOTIFICATION DATE		DELIVERY MODE		
06/24/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/729,239

Applicant(s)

SWOBODA, GARY L.

Examiner

Stephen J. Cherry

Art Unit

2863

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 April 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16 is/are allowed.
- 6) ☐ Claim(s) 1-3, 5, 7-15 is/are rejected.
- 7) ☒ Claim(s) 4 and 6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-893)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4-23-2008 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: an element that provides timing trace streams during primary code execution, upon which continued operation, as claimed at line 5 of claim 1, is based.

Regarding claim 3, the phrase "can have" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,859,891 to Edwards et al in view of U.S. Patent 3,659,272 to Price et al.

With regard to claim 1, Edwards discloses a trace apparatus comprising:
a trigger unit responsive to user and target processor state input signals, the trigger unit generating control signals in response to the input signals ('891, col. 8, line 8 and fig. 1, ref. 103);
timing trace apparatus, ('891, col. 8, line 58);
program counter and data trace apparatus ('891, col. 6, line 45 and col. 7, line 4 and col. 8, line 58) and

a test and debug port, the test and debug port adapted for coupling to a communication bus, the test and debug port receiving signal from and sending signals to a host processor unit ('891, fig. 4, connections of ref. 401 and 402 to link, 420).

Edwards does not explicitly recite selectively providing trace streams in secondary code, while continuing to provide timing trace streams during primary code execution.

The claims further recite selectively providing trace streams in secondary code, while continuing to provide timing trace streams during primary code execution, as disclosed by Price ('272, col. 2, line 4, with secondary code the "new procedure", at line 18, and primary code the "prior procedure, at line 31).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the selectable trace of Price with the invention of Edwards to allow program debugging in a computer ('272, col. 1, line 12).

With regard to claim 2, and in view of the rejection of claim 1 above, Price discloses a apparatus as recited in claim 1 wherein secondary code execution is background or interrupt service routine code execution ('272, col. 2, line 18, "new procedure", executed, then returned to background at line 32, "return after having completed execution of the new procedure").

With regard to claim 3, and in view of the rejection of claim 1 above, Edwards discloses a trace apparatus as recited in claim 1 wherein the target processor can have one of an unprotected pipeline and a protected pipeline ('891, col. 5, line 62).

With regard to claim 5, Price discloses an apparatus as recited in claim 1 wherein the target processor has three states, a primary code execution state ('272, col. 2, line 31, "prior procedure"), a secondary code execution state ('272, col. 2, line 18, "new procedure"), and an execution halt state ('272, col. 5, line 2, "trace interrupt procedure", where the prior procedure and new procedure are not executed, therefor, halted); and wherein the trigger unit is responsive to the three states to selectively enable and disable traces ('272, col. 2, line 4), and Edwards discloses traces with timing, program counter, and data trace ('891, col. 6, line 45 and col. 7, line 4 and col. 8, line 58).

Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,859,891 to Edwards et al in view of U.S. Patent 3,659,272 to Price et al.

With regard to claim 7, Edwards discloses a method of generating trace streams in a target processor for transmission to a host processor, the method comprising: generating a timing trace stream, ('891, col. 8, line 58); a program counter trace stream and data trace stream ('891, col. 6, line 45 and col. 7, line 4 and col. 8, line 58) and sending the trace streams to a host processing unit over a communication bus ('891, fig. 4, connections of ref. 401 and 402 to link, 420).

Edwards does not explicitly recite selectively providing trace streams in secondary code, while continuing to provide timing trace streams during primary code execution.

The claims further recite selectively providing trace streams in secondary code, while continuing to provide timing trace streams during primary code execution, as disclosed by Price ('272, col. 2, line 4, with secondary code the "new procedure", at line 18, and primary code the "prior procedure", at line 31).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the selectable trace of Price with the invention of Edwards to allow program debugging in a computer ('272, col. 1, line 12).

With regard to claim 8, and in view of the rejection of claim 7 above, Edwards discloses a method as recited in claim 7 further comprising including in the target processor input signals indicia of the state of the target processor, the target processor having a primary code execution state, a secondary code execution state and an execution halt state ('891, col. 9, line 66).

With regard to claim 9, and in view of the rejection of claim 7 above, Edwards discloses a method as recited in claim 7 further comprising including in the target processor input signals indicia indicating whether the target processor was in a protected pipeline mode of operation or in an unprotected pipeline mode of operation ('891, col. 9, line 66, "stall" signal refers to pipeline mode of operation).

With regard to claim 10, and in view of the rejection of claim 7 above, Edwards discloses a method as recited in claim 7 further comprising including in the user input

signals whether the timing trace was enabled during instruction execution halts ('891, col. 8, line 61, and col. 10, line 64).

With regard to claim 11, and in view of the rejection of claim 9 above, Edwards discloses a method as recited in claim 9 further comprising including in the user input signals identifying when the timing trace stream was enabled during the secondary code execution state ('891, col. 8, line 61, and col. 10, line 64).

Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,859,891 to Edwards et al in view of U.S. Patent 3,659,272 to Price et al.

With regard to claim 12, Edwards discloses a processing unit comprising: a trigger unit responsive to user and target processor state input signals, the trigger unit generating control signals in response to the input signals ('891, col. 8, line 8 and fig. 1, ref. 103); timing trace stream generation unit, ('891, col. 8, line 58); program counter generation and data trace stream generation unit ('891, col. 6, line 45 and col. 7, line 4 and col. 8, line 58) and a port for applying selected trace signal to a communication bus ('891, fig. 4, connections of ref. 401 and 402 to link, 420).

Edwards does not explicitly recite selectively providing trace streams in secondary code, while continuing to provide timing trace streams during primary code execution.

The claims further recite selectively enabling and disabling tracing in response to a state of operation, and primary, secondary ('272, col. 2, line 4), and halted execution states ('272, col. 5, line 2, "trace interrupt procedure", where the prior procedure and new procedure are not executed, therefor, halted).

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the selectable trace of Price with the invention of Edwards to allow program debugging in a computer ('272, col. 1, line 12).

With regard to claim 13, and in view of the rejection of claim 12 above, Price discloses enabling tracing in secondary code execution ('272, col. 2, line 23), and Edwards discloses timing trace generation ('891, col. 8, line 8, and col. 9, line 66).

With regard to claim 14, and in view of the rejection of claim 13 above, Edwards discloses a processing unit as recited in claim 13 wherein second control signals enable the timing trace generation device and the program counter and data trace generation units during the secondary code execution ('891, col. 8, line 8, and col. 9, line 66).

With regard to claim 15, and in view of the rejection of claim 12 above, Edwards discloses a processing unit as recited in claim 12 including indicia of a protected pipeline mode of operation and of an unprotected mode of operation of the central processing unit are part of the central processing unit input signals ('891, fig. 4, "stalled", 410, indicates whether pipeline is protected from overfilling buffer).

Allowable Subject Matter

Claim 16 is allowed.

The following is an examiner's statement of reasons for allowance:

Claim 16 recites, "a pipeline flattener, the pipeline flattener aligning the program counter address with the completion of the instruction, the pipeline flattener flushing instructions in response to a halt execution signal in an unprotected pipeline, the pipeline flattener halting operation in a protected pipeline". This feature, in combination with the remaining structure, overcomes the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims 4 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if the objection of the base claim described above is overcome.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 4 recites, "a pipeline flattener, the pipeline flattener aligning the program counter address with the completion of the instruction, the pipeline flattener flushing instructions in response to a halt execution signal in an unprotected pipeline, the

pipeline flattener halting operation in a protected pipeline". This feature, in combination with the remaining structure, overcomes the prior art of record.

Claim 6 recites, "wherein the timing trace stream can be controllably enabled during an execution halt state". This feature, in combination with the remaining structure, overcomes the prior art of record.

Response to Arguments

Applicant's arguments with respect to claims 1-3, 5, and 7-15 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen J. Cherry whose telephone number is (571) 272-2272. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJC

/John E Barlow Jr./
Supervisory Patent Examiner, Art
Unit 2863

